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10/619,136

07/14/2003

David Mark

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06/30/2004

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EXAMINER

NGUYEN, JIMMY

ART UNIT

PAPER NUMBER

2829

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/619,136

Applicant(s)

MARK ET AL.

Examiner

Jimmy Nguyen

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 0604.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 11, 13, 14 , 17 – 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Nicolai (US 5198707).

**As to claim 1**, Nicolai (fig 1) disclose a test configuration comprising:

An IC (connected to pin 10, column 2 line 65) to be tested;

An i/o pad (10) of the ic (connected to pin 10, column 2 line 65);

A current injector (12) on the IC (connected to pin 10, column 2 line 65) coupled between the i/o pad (10) for injecting a current at the i/o pad; and

A detector (switches and resistors) on the IC (connected to pin 10, column 2 line 65) for detecting a logic level of the i/o pad (10).

**As to claims 2, 3**, Nicolai (fig 1) disclose a test configuration comprising an output buffer, wherein an output terminal of the output buffer s coupled to the i/o pad and is tri-state buffer.

**As to claim 4,** Nicolai (fig 1) disclose a test configuration comprising an input buffer, wherein an input terminal of the input buffer is coupled to the i/o/ pad (10).

**As to claim 5,** Nicolai (fig 1) disclose a test configuration comprising the current injector (12) is selectively enabled by a memory bit (predriver).

**As to claim 6,** Nicolai (fig 1) disclose a test configuration wherein the current injector (12) is a resistive element on the ic coupled between the i/o/ pad (10) and Vcc.

**As to claim 7,** Nicolai (fig 1) disclose a test configuration wherein the resistive element is a transistor (plurality of switches).

**As to claim 8,** Nicolai (fig 1) disclose a gate of the transistor (plurality of switches) is coupled to a memory bit (register 16).

**As to claims 9, 10,** Nicolai (fig 1) disclose the voltage reference node is a power node (Vcc) and ground node.

**As to claim 11**, Nicolai (fig 1) disclose IC is one of plurality of IC on a wafer.

**As to claim 13**, Nicolai (fig 1) disclose the IC is a programmable logic device.

**As to claim 14**, Nicolai (fig 1) disclose the detector (resistors and plurality of switches) is a boundary scan cell.

**As to claims 17 - 26**, Nicole (fig 1) and Yanagawa et al (fig 2) disclose a test configuration In *In re King*, 801 F.2d 1324, 1326 USPQ 136, 138 (Fed. Cir. 1986) it was held that: "Under the principles of Inherency, if a structure in the prior art necessarily functions in accordance with the limitations of a process or method claim of an application, the claim is anticipated." The court added, however, that: "This is not to say that the discovery of a new use for an old structure based on unknown properties of the structure might not be patentable to the discoverer as a process. *In re Hack*, 245 F.2d 246, 248, 114 USPQ 161, 163 (CCPA 1957)."

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nicolai (US 5198707) in view of Yanagawa et al (US 6348810).

**As to claim 12**, Nicolai (fig 1) disclose the structure of a test configuration except for a probe card coupled to subset of the plurality of I/O pads; and ate coupled to the probe card.

On the other hand, Yanagawa et al teach (fig 2) a probe card (28) coupled to subset of the plurality of I/O pads (21); and ate (24) coupled to the probe card (28).

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the test structure of Nicole and use the probe card with ate of Yanagawa for the purpose of testing numerous IC device at the same time.

***Allowable Subject Matter***

5. Claims 15, 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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The prior art of record do not disclose a test configuration further comprising a second transistor coupled between the input pad and a ground node;

A memory bit coupled to a gate of the first transistor; and

A memory bit coupled to a gate of the second transistor.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Nguyen at (703) 306-5858. Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4900.

JN.  
June 26, 2004

*David A. Zamek*  
David A. Zamek  
Primary Examiner  
6/26/04